IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Hapke**
Application No.	:	**09/923,604**
Filed	:	**August 7, 2001**
For	:	**ARRANGEMENT AND METHOD OF TESTING AN INTEGRATED CIRCUIT**

APPEAL BRIEF

On Appeal from Group Art Unit 2133

Date: September 6, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

Certificate of Fax/Mailing Under 37 CFR 1.8

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Daniel Michalek
(Name)

6-Sep-05
(Signature and Date)

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TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-3 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a test arrangement and a test method which allows for the testing of edge transitions of a combinational system using a relatively simple combinational test sample generator. Two test clock cycles are executed with only one test vector being provided for both test clock cycles. The vector consecutively

runs through the combinational system twice. The test vector only needs to be read once at the end of the second test clock cycle. Figure 1 illustrates the test arrangement. Figure 2 illustrates conceptually test software used to check the test results. Conceptually, first and second identical software models 11 and 16 are arranged in series such that the second software model operates upon the results of the first software model.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-3 are unpatentable over Kasayu in view of Patel and further in view of Hamzaoglu.

VII. ARGUMENT

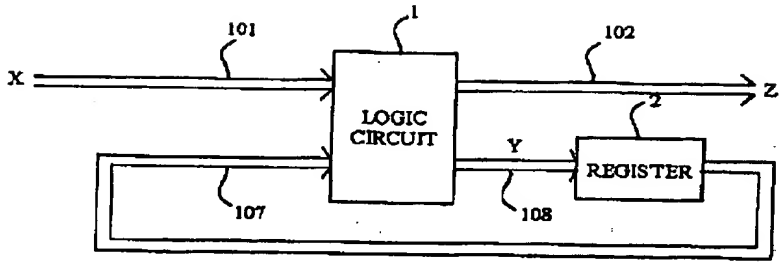
I. Rejection of Claims 1-3 as unpatentable over Kasaya in view of Patel and further in view of Hamzaoglu

Kasuya discloses a test arrangement for performing at-speed test of an integrated circuit without requiring pre-computed test vectors.

The Final Rejection states in part:

> The test circuit [of Kasuya], in a test mode, applies a first test sample in a first test clock cycle to the input of the combination al logic system of the integrated circuit, and receives the output signal in a buffer memory, and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combination logic system and again receives the output signal of the combinational logic system in the buffer memory, the buffer circuit being constituted as a shift register. (References omitted.)

Referring to the cover figure of Kasuya, the portion of the circuit illustrated below is a conventional sequential logic circuit:



In a conventional sequential logic circuit of this type, inputs X to the logic circuit 1 together with the previous output Y of the logic circuit 1 determine the next outputs Y, Z of the logic circuit 1. Feedback of the outputs Y is part of the normal operation of the sequential logic circuit, or "state machine."

The remainder of the circuit not illustrated above is provided for testing purposes.

In test mode, however, the feedback path from the register back to the input of the logic circuit is not operative. Note for example Figure 4, illustrating the circuit in its test configuration, and the lack of any feedback from the output of the logic circuit to the input of the logic circuit. Localized feedback may be employed within the signal sequence compressor 204, but this type of feedback is distinct from the feedback claimed as part of the present invention.

It may be seen therefore that Kasuya does not in fact teach what the Office Action describes it as teaching. Nor does it teach or suggest the present invention as claimed.

These deficiencies of the primary reference Kasuya are not remedied by the secondary references. Accordingly, the references cannot be said to render obvious the invention recited in claims 1 and 3.

With regard to dependent claim 2, this claim depends from independent claim 1, which has been shown to be patently distinguishable over the cited references. Accordingly, claim 2 is also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. An arrangement for testing an integrated circuit comprising a combinational logic system and a test circuit, which arrangement performs a test of the behavior of the combinational logic system in comparison with test software which emulates the nominal behavior of the integrated circuit, the arrangement comprising:

two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;

wherein the test circuit, in a test mode, applies a first test sample in a first test clock cycle to the input of the combinational logic system of the integrated circuit and [takes over] receives the output signal in a buffer memory and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combinational logic system and again receives the output signal of the combinational logic system in the buffer memory

wherein, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory with the results of the second software model.

2. An arrangement as claimed in claim 1, characterized in that the buffer memory is constituted as a shift register by means of which the test samples are read and/or written.

3. A method of testing an integrated circuit comprising a combinational logic system and a test circuit, in which method the behavior of the combinational logic system is compared with test software which emulates the nominal behavior of the integrated circuit, the method comprising:

providing two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;

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X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

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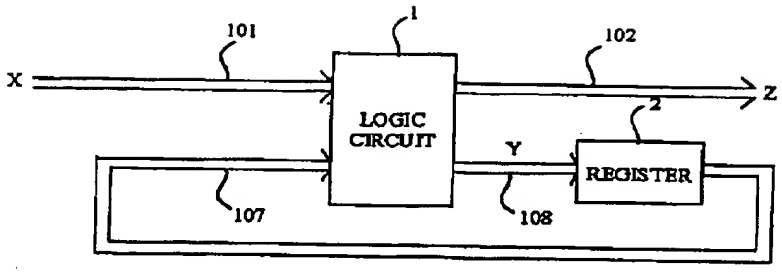

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